REMARKS

A telephone conference between the Examiner and Dennis Smid (one of the applicant's undersigned attorneys) was held on June 30, 2004. The applicant and Mr. Smid wish to thank the Examiner for his time and consideration for such telephone interview.

It is submitted that these claims, as originally presented, are patentably distinct over the prior art cited by the Examiner, and that these claims were in full compliance with the requirements of 35 U.S.C. §112. Changes to these claims, as presented herein, are not made for the purpose of patentability within the meaning of 35 U.S.C. §101, §102, §103 or §112. Rather, these changes are made simply for clarification and to round out the scope of protection to which Applicant is entitled.

Claims 2, 4-7, and 9, amended claims 1,3, and 8, and new claims 10-20 are in the application.

Claims 1 and 3 were rejected under 35 U.S.C. 112, first paragraph, "because the specification, while being enabling for the decimation filtering of the sum path is used for the sampling rate decimation of the stereo-sum signal $m_s(t)$ and the pilot carrier, see Applicant's specification on page 7 lines 26-31, does not reasonably provide enablement for the PLL, receiving the sampling rate decimated stereo-sum signal $m_s(t)$ as input signal, which is sampling rate decimated....it is evident that the sampling rate decimation filter 5 filters and decimates both the stereo-sum signal ms(t) and the pilot carrier, and the output signal of the sampling rate decimation filter 5, comprises both the stereo-sum signal ms(t) and the pilot carrier, is inputted to a DPLL 4 in contrast with the claim that PLL circuit receives the sampling rate decimated stereo-sum signal ms(t) as input signal." Claims 4-9 were also rejected due to dependency on claim 3.

As discussed during the June 30th conference, and contrary to the Examiner's position, it is respectfully submitted that the output of decimation filter 5 is the stereo-sum ms(t) signal, as clearly indicated in Fig. 1 of the present application. Such stereo-sum ms(t) signal does **not**

include the pilot signal, as clearly defined by the equation for the stereo-sum signal set forth on line 13 of page 2 of the present application. As a result, the signal inputted to the DPLL 4 of Fig. 1 is the stereo-sum signal ms(t) (which does not include the pilot signal).

Therefore, it is respectfully requested that the above 112 rejections of claims 1, and 3-9 be withdrawn.

Claims 1, 3, and 8 were rejected under 35 U.S.C. 112, second paragraph. In explaining these rejections, the Examiner appears to assert that the phrase "and/or" and the word "or" renders the claims indefinite. During the June 30th conference, the Examiner stated that the phrase "and/or" should be changed. In response thereto, the phrase "and/or" in claims 1, 3, and 8 has been changed to "or" and new claims 10-20 have been added herein. Also, during the June 30th conference, the Examiner stated that the word "or" is acceptable.

Claims 1-2 were rejected under 35 U.S.C. 102(b) as being anticipated by Reich, U.S. Patent 4,827.515. Claim 3 was rejected under 35 U.S.C. 103(a) as being unpatentable over Reich, U.S. Patent 4,827,515 as applied to claim 1.

In explaining the above 102 rejection of claim 1, the Examiner stated that the digital demodulator of Fig. 1 of Reich "includes a phase-locked loop in the form of a variable oscillator, the carrier conditioning circuit tr, one of the five carriers t1-t5 with the respective associated low-pass filter b1-b4, b6, and the control signal st. Output of the second decimation circuit d2, namely ds', containing the stereo-sum signal ss and the pilot signal ps, is inputted to the phase-locked loop...." (See line 22 of page 5 to line 4 of page 6 of the present office action.)

Claim 1 recites in part the following:

> "wherein said PLL-circuit **receives the sampling rate decimated stereo-sum signal ($m_s(t)$) as input signal**, which is sampling rate decimated by a decimation factor of D." (Underlining and bold added for emphasis.)

Accordingly, the PLL-circuit of claim 1 receives the stereo-sum signal as an input signal. In the demodulator of Reich, on the other hand, the input to its PLL circuit (oscillator vo) is a control signal st. As clearly shown in Fig. 1 of Reich, the stereo-sum ss is not supplied to its oscillator vo. Thus, Reich does not appear to disclose the above features of claim 1.

Therefore, it is respectfully submitted that claim1 and claim 2 dependent therefrom are distinguishable from Reich as applied by the Examiner. For reasons similar to those previously described with regard to claim1, it is also respectfully submitted that claim3 is distinguishable from Reich as applied by the Examiner. Furthermore, the Examiner acknowledged that Reich does not show "a recovered pilot carrier which is interpolated..." as in claim 3.

In the event, that the Examiner disagrees with any of the foregoing comments concerning the disclosures in the cited prior art, it is requested that the Examiner indicate where, in the reference or references, there is the basis for a contrary view.

In view of the foregoing amendments and remarks, it is believed that all of the claims in this application are patentable over the prior art, and early and favorable consideration thereof is solicited.

Please charge any lees incurred by reason of this response and not paid herewith to Deposit Account No. 50-0320.

Respectfully submitted,

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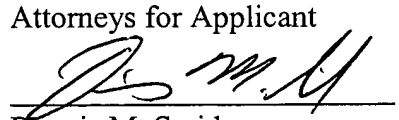
By: 

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